Amendments to the Written Description of the Specification

Applicant presents replacement paragraphs below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

On page 1, after the title insert: --Background Of The Invention--;

On page 1, after "Background of the Invention" but before the first paragraph insert --1. Field of the Invention--;

On page 1, before the second paragraph beginning on line 10, insert --2. Discussion of the Related Art--;

Please replace the second paragraph on page 1, lines 8-12 as shown:

--~~Such a~~ A TFA sensor (Thin Film on ASIC (TFA) Technology) comprises a matrix-organized or linear arrangement of pixels. The electronic circuits for operating the sensor (e.g. pixel electronics, peripheral electronics, system electronics) are usually realized using CMOS-based silicon technology and form an application specific integrated circuit (ASIC).—

Please replace the third paragraph on page 2, lines 8-15 as shown:

--A typical layer configuration is disclosed in the patent application TFA image sensor with extremely low dark current ~~(file reference 10063837.6)~~, U.S. Serial No. 10/541,440. Furthermore, detector structures with a controllable spectral sensitivity are known (P. Rieve, M. Sommer, M. Wagner, K. Seibel, M. Böhm, a-Si:H Color Imagers and Colorimetry, Journal of Non-Crystalline Solids, vol. 266-269, pp. 1168-1172, 2000). This basic structure of a TFA image sensor can furthermore be extended by additional, upstream layers in the direction of light incidence, for example by color filter layers (e.g. Bayer pattern, US patent No. 3971065).--

On page 4, before line 4, insert --Summary of the Invention--;

On page 4, before line 19, insert --Brief Description of the Drawings

Fig. 1 is an illustration of a pin;

Fig. 2 is an illustration of a Schottky photodiode;

Fig. 3 illustrates the initial state before the beginning of the TFA processing;

Fig. 4 illustrates the state after the removal of the conductive layer of the topmost metallization;

Fig. 5 illustrates the result after the patterning of the lower barrier layer;

Fig. 6 illustrates the pixel back electrodes coated with the multilayer system comprising amorphous silicon and TCO;

Fig. 7 illustrates a process variant;

Fig. 8 illustrates another process variant;

Fig. 9 illustrates still a further process variant;

Fig. 10 illustrates the further metal layer deposited directly onto the intermetal dielectric forming the pixel back electrodes after patterning; and

Fig. 11 illustrates the photodiode-forming layers applied to the pixel back electrodes after patterning.--

On page 4, before line 19, insert --Detailed Description--;